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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 5 (Cancelled):

Claim 6. (Original): A compression engine comprising:

an input port for receiving input data vectors;

an output port for providing codevectors and an index map;

volatile memory in data communication with the input port and the output port for storing the input data vectors, the codevectors and the index map;

a codevector trainer in data communication with the volatile memory for training codevectors in dependence upon the input data vectors using one of along vector components codevector training or across vector components codevector training; and,

a controller in communication with the codevector trainer and the volatile memory for executing in cooperation with the codevector trainer one of SAMVQ or HSOCVQ data compression in order to produce compressed data comprising the codevectors and the index map.

Claim 7. (Original): A compression engine as defined in claim 6 comprising a programming bus connected to a programming port, the codevector trainer, the controller, and the volatile memory for transmitting a control signal.

Claim 8. (Original): A compression engine as defined in claim 7 wherein the codevector trainer comprises hardware units for executing one of along vector components codevector training and across vector components codevector training in dependence upon a received control signal.

Claim 9. (Original): A compression engine as defined in claim 8 wherein the controller

is capable of executing either one of a Successive Approximation Vector Quantization or a Hierarchical Cluster Vector Quantization.

Claim 10. (Original): A compression engine as defined in claim 9 wherein the data compression is performed within the compression engine without external communication during the compression process.

Claim 11. (Original): A compression engine as defined in claim 10 comprising a clock domain decoupled from a clock domain of a system environment with which it is in communication.

Claim 12. (Original): A compression engine as defined in claim 11 wherein the hardware components of the compression engine are accommodated within a single IC.

Claim 13. (Original): A compression engine as defined in claim 12 wherein the IC is a FPGA.

Claims 14 - 28 (Cancelled):